## REMARKS

Claims 1 through 39 are currently pending in the application.

Claims 40 through 44 have been canceled.

This amendment is in response to the Office Action of June 21, 2000.

Claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nakashima (United States Patent 5,661,086).

Claims 2 through 4, 15 through 17 and 28 through 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima (United States Patent 5,661,086) as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43, and further in combination with Fujimoto (United States Patent 5,773,896).

Claims 5, 6, 8 through 11, 18, 19, 21 through 24, 31, 32 and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43 and further in combination with Applicant's admitted prior art.

Claim 44 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33, and 38 through 43 and further in combination with Pavio (United States Patent 5,528,076).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, applicant has amended claims 1, 14, 27, and 40 to clearly distinguish over the cited prior art. Claims 20, 31 and 33 were amended to correct minor errors in the text.

**35 U.S.C. § 102(b) Anticipation Rejections**

Claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nakashima (United States Patent 5,661,086). Applicant has amended independent claims 1, 14, 27, and 40 to more clearly distinguish the claimed invention over the prior art. Applicant traverses the rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Nakashima teaches a semiconductor device assembly in which a metal substrate 12 serves as a support for a circuit substrate 17 and a semiconductor die 14. Metal substrate 12 is taught to have favorable heat conductivity (col. 8, lines 14-15), and is provided with a square die mounting region 11 (col. 8, lines 24-25), a first pair of side rails 31 (col. 8, line 24), and a plurality of connecting tabs 32, 32*a* on each of the four sides of metal substrate 12 (col. 8, lines 31-32). A plurality of metal substrates 12 may be connected in series by side rails 31 and connecting tabs 32, 32*a* (col. 8, lines 22-33). A circuit substrate 17 is adhered to each metal substrate 12 by means of prepreg layer 15*a* (col. 6, lines 26-27). Circuit substrate 17 is provided with an opening/cavity 18 at its center portion for receiving a semiconductor die 14 (col. 6, line 33). Circuit substrate 17 is made of a "glass fabrics reinforced epoxy resin", and is configured with a mounting face 16 for mounting circuit substrate 17 to a printed wiring board (PWB) (col. 6, lines 46-47). Mounting face 16 is taught to be configured with a solder resist layer 23, conductive leads 21 with wire bonding pads 19 and terminal pads 20 on respective ends thereof, and a plurality of solder balls 24 mounted on terminal pads 20 and forming a ball grid array (BGA) (col. 6, lines 55-63, and col. 7, lines 1-20). A semiconductor die 14 is accommodated in opening/cavity 18 and adhered to die mounting region 11 of metal substrate 12 by an electrically conductive adhering agent layer 26*a* (col 6, lines 32-34). Wire bonding pads 19 are connected with corresponding electrode pads 13 on semiconductor die 14 by bonding wires 25 (col. 6, lines 65-67 through col. 7, line 1). A potting resin 26 made of epoxy oriented resin is filled in cavity 18 to seal semiconductor die 14, bonding wires 25, and the inner ends of conductive leads 21 (col. 7, lines 21-25). Potting resin 26 is taught to "be sufficiently lower than the solder ball 24 in height so that the solder balls 24 can sufficiently protrude downwardly to be reliably connected with the PWB" (col. 7, lines 25-28).

Applicant first submits that claims 1, 7, 12-14, 20, 25 through 27, 33, 38, and 39 of the presently amended invention are not anticipated by the Nakashima reference because Nakashima does not explicitly or inherently describe each and every element of independent claims 1, 14, and 27. More specifically, Nakashima does not describe the elements of: "at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said

semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump" (claim 1); "at least one projection secured to at least one bond pad on said active surface of said semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump" (claim 14); "a plurality of projections connected to said plurality of bond pads for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps" (claim 27). (Emphasis added). The claim amendments adding the terms ". . . including one of at least one solder ball and at least one solder bump" or ". . . including one of a plurality of solder balls and a plurality of solder bumps" and "direct" in relation to the recitation of "projections" and "connection", respectively, are supported by applicant's disclosure in the *Specification* on page 3, lines 15 through 21, and page 6, lines 6 through 9, and by applicant's *Drawings* in FIGs. 4 and 5.

In contrast to the limitations of the present invention, Nakashima teaches a metal substrate 12 for mounting both a semiconductor die 14 and a circuit substrate 17 wherein semiconductor die 14 is connected to circuit substrate 17 by means of intervening wirebonding interconnections 25 which are mounted on wire bonding pads 19 of die 14 (presumably by conventional soldering techniques). (Nakashima, col. 6, lines 65-67, and col. 11, lines 48-53).

Since Nakashima does not describe the above-mentioned claim limitations reciting projections proximately disposed on bond pads on the active surface of a semiconductor die for direct connection to a substrate or a host circuit board, the projections comprising one of a solder ball or solder bump (independent claims 1, 14, and 27) Applicant respectfully submits these claims are not anticipated by Nakashima. Furthermore, since independent claims 1, 14, and 27 are allowable, the dependent claims therefrom are allowable. Applicant respectfully requests that the anticipation rejections under the provisions of 35 U.S.C. § 102 be withdrawn and that claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38 and 39 allowed.

**35 U.S.C. § 103(a) Obviousness Rejections**

Claims 2 through 4, 15 through 17 and 28 through 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima (United States Patent 5,661,086) as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43, and further in combination

with Fujimoto (United States Patent 5,773,896). Claims 5, 6, 8 through 11, 18, 19, 21 through 24, 31, 32 and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakashima as applied to claims 1, 7, 12 through 14, 20, 25 through 27, 33 and 38 through 43 and further in combination with Applicant's admitted prior art. Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The teachings of Nakashima have been previously discussed. The Examiner stated that Fujimoto teaches a plurality of projections 22 on a semiconductor die which comprise a BGA (Office Action, page 3). The Examiner also thought that the product of claims 5, 6, 8-11, 18, 19, 21-24, 31, 32, and 34-37 (relating to the adhesive layer) was admitted by the applicant to be well known in the prior art (*Id.*).

Applicants submit that the 35 U.S.C. § 103(a) obviousness rejections of claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 should be withdrawn because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the Nakashima reference or to combine the reference with the teachings of Fujimoto (the first element of a *prima facie* case for obviousness). Applicant further submits that there could be no reasonable expectation in the combination of references (the second element of a *prima facie* case for obviousness).

As previously discussed, Nakashima teaches a large metal substrate 12 for accommodating both a centrally positioned semiconductor die 14 and a PWB-interconnecting circuit substrate whose perimeter region surrounds the die 14 on all four sides (Nakashima, col. 6, lines 10 through 32; see also FIG's. 1 through 3, 11, and 12). Applicants submit that one of

skill in the art would not be motivated to combine the flip-chip taught by Fujimoto with the teachings of Nakashima because Nakashima contrastingly teaches that solder balls on 24 on circuit substrate 17, rather than on die 14, form the basis for external communication with other components. (Nakashima, col. 7, lines 1 through 29). Since external communication is already accomplished by means of solder balls 24 on circuit substrate 17, there is no teaching or suggestion to replace die 14 with the flip-chip of Fujimoto.

Furthermore, die 14 of Nakashima is taught to be mounted in die mounting region 11 of metal substrate 12 such that potting resin 26 is "sufficiently lower than the solder ball 24 in height so that the solder balls 24 can sufficiently protrude downwardly to be reliably connected with the PWB." (Nakashima, col. 7, lines 25 through 28). Thus, modifying the teachings of Nakashima and Fujimoto to that of the present invention would also require a teaching or suggestion to eliminate circuit substrate 17, the consequence of which would also eliminate the need for metal substrate 12 which serves primarily as a support structure for both circuit substrate 17 and die 14. (Nakashima, col. 4. lines 38 through 49).

Further in this regard, Nakashima teaches that circuit substrate 17 is integral to his semiconductor device assembly in that the BGA thereon forms the basis for external communication with other components. (Nakashima, col. 7, lines 1 through 29). Applicant thus submits that to eliminate circuit substrate 17 would impermissibly change the principle of operation of the invention set forth in the reference.

> "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." M.P.E.P. §2143.01 (citing *In re Ratti*, 123 USPQ 349 (CCPA 1959)).

As additional support for the nonobviousness of the present invention, Applicant submits that the present invention omits the Nakashima element of circuit substrate 17 while retaining its interconnection function by use of a semiconductor die with flip-chip-type interconnection capability. See *In re Edge*, 359 F.2d 896, 149 USPQ 556 (CCPA 1966) and MPEP § 2144.04.

Finally, Applicant submits that there could be no reasonable expectation of success in the combination because replacing die 14 with the flip-chip taught by Fujimoto would result in the flip-chip being placed into cavity 18 of circuit substrate 17. This would result in a

semiconductor die with no suitable means for external communication, thus conflicting with elements of claims 1, 14, and 27 which are essentially directed to projections on the active surface of a semiconductor die for direct connection to a substrate.[1] The following element of claim 1 is representative of similar elements in claims 14 and 27 which are directly contradictory to the hypothetical product of the combination of cited references, "at least one projection proximately connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate".

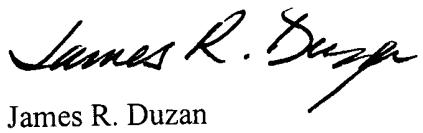
The nonobviousness of independent claims 1, 14, and 27 precludes a rejection of claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 which depend therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Accordingly, applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 103(a) obviousness rejections to claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37.

[1]No suitable means for external communication for the die would exist since Nakashima teaches that die 14 is mounted to die mounting region 11 of metal substrate 12 such that potting resin 26 is "sufficiently lower than the solder ball 24 in height so that the solder balls 24 can sufficiently protrude downwardly to be reliably connected with the PWB." (Nakashima, col. 7, lines 25-28).

## CONCLUSION

Applicant respectfully requests the allowance of claims 1 through 39 and the case passed for issue. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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## APPENDIX A

1. (Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a paddle of a lead frame of a plurality of lead frames having side rails connected to said paddle, said second surface of said semiconductor die secured to said paddle.

14. (Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface;

at least one projection secured to said at least one bond pad on said active surface of said semiconductor die for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a metal paddle from a lead frame, said second surface of said semiconductor die attached to said metal paddle.

20. (Amended) The semiconductor device assembly of claim 14, further comprising:

an electrically conductive adhesive layer attaching said second surface to said metal paddle.

27. (Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

a plurality of projections connected to said plurality of bond pads for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die.

31. (Amended) The semiconductor device assembly of claim 27, further comprising: an electrically non-conductive adhesive layer connecting said second surface to said metallic paddle.

33. (Amended) The semiconductor device assembly of claim 27, further comprising: an electrically conductive adhesive layer connecting said second surface to said metallic paddle.